

**Title: Forward Error Correction (FEC) on a Link
Between ICs**

5 Field of the Invention

The present invention relates generally to high-speed transport networks and, more particularly, to the transmission of signals on backplanes and between ICs on a same circuit pack using error correction techniques for reducing bit error rates at high transmission speeds.

15 Background

At relatively low speeds of data transportation, roughly 100 Mb/sec, error rates between two different ICs on a circuit pack or over a backplane are generally unmeasurable. In other words, they are close to zero. As speeds of data transportation over backplanes and between ICs increase to 2.5 Gb/s and above, the likelihood of having transmission errors increases as well. These errors may be due to effects such as inter-symbol interference, attenuation, couplings between links on the ICs, noise coupling from digital to analog section of an IC, simultaneous switching noise in ICs, signal distortion in connectors or backplane, and process distortion, among others. Consequently, it becomes difficult to get sufficiently low errors rates.

Consequently, there is a need in the industry for reducing bit error rates at high transmission speeds over backplanes and between ICs.

Summary of the Invention

5 In accordance with a broad aspect, the invention provides the use of forward error correction data in a signal carried over a link between two ICs (Integrated Circuits). In a non-limiting example, the link between two ICs is between two ICs on a same circuit pack. 10 Alternatively, the link between two ICs includes a backplane.

In a specific example, the link between two ICs is a medium suitable for the propagation of electrical signals. 15

In accordance with another broad aspect, the invention provides a method for generating a signal for transmission over a link between two ICs. An input signal is received, the input signal comprising payload data to be transmitted 20 over the link between two ICs. The data in the input signal is processed to derive forward error correction data at least on part on the basis of the payload data in the input signal. An output signal comprising the payload data received in the input signal and the forward error 25 correction data is then generated and released for transmission over the link between two ICs.

In a specific example, the link between two ICs can include a backplane or a link between two ICs on a same 30 circuit pack.

In accordance with another broad aspect, the invention provides an apparatus for implementing the above-described method.

5 In accordance with another broad aspect, the invention provides a signal carried over a link between two ICs. The signal includes a sequence of frames, each frame including a plurality of sequential blocks, each block being characterized by a compound data structure suitable for carrying payload data and overhead information. The
10 compound data structure is derived by bit-multiplexing a set of N primary data structures. Each primary data structure comprises a first portion and a second portion, the first portion including payload data, the second
15 portion including forward error correction data derived from the data elements in the first portion.

In a non-limiting specific example of implementation, the signal has a rate of about 2.5 Gb/s and comprises a
20 sequence of frames, each frame includes 1 framing pattern and 66 sequential blocks. Each block being characterized by a compound data structure, where the compound data structure is derived by bit-multiplexing a set of 4 primary data structures. In other words $N=4$. The skilled person in
25 the art will readily appreciate that N can take on a plurality of non-negative integer number values greater than 0. In a non-limiting example, N is selected from the set consisting of {1, 2, 3, . . . , 14, 15, 16}. Each primary data structure includes about 1176 bits, wherein at
30 least part of the first 1164 bits of each primary data structure includes payload data, and 12 bits include forward error correction.

It will be readily appreciate that any suitable coding may be applied to the payload data in a given block to derive the forward error correction data for that given block. In a very specific non-limiting example, the forward error correction data in a given primary data structure are derived by applying BCH-1 coding on at least part of the payload data of the given primary data structure. The skilled person in the art will readily appreciate that methods, other than BCH-1 coding, may be used in connection with FEC without detracting from the spirit of the invention.

In accordance with another broad aspect, the invention provides a method and an apparatus for generating the above-described signal for transmission over a link between two ICs. The link between two ICs may include a backplane or a link between two ICS on a same circuit pack.

In accordance with another broad aspect, the invention provides an IC suitable for processing a signal of the type described above. Processing a signal comprises plurality of signal processing functions including but not limited to signal generation and signal information extraction.

Other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

Brief Description of the Drawings

Fig. 1 is a specific example of an apparatus for generating a signal constructed in accordance with a specific example of implementation of the invention;

5

Fig. 2 is a detailed block diagram of the processing unit in the apparatus of figure 1;

Fig. 3 depicts a primary data structure in accordance with a specific example of implementation of the invention;

Fig. 4 shows a compound data structure in accordance with a specific example of implementation of the invention;

Fig. 5 depicts a signal characterized by a digital signal frame format providing forward error correction in accordance with a specific example of implementation of the invention;

Fig. 6 is a specific example of an apparatus for extracting information from a signal constructed in accordance with a specific example of implementation of the invention;

Fig. 7 is a detailed block diagram of the processing unit in the apparatus of figure 6;

Fig. 8 is a block diagram of a specific example of implementation of the apparatuses of figures 1 and 6.

In the drawings, embodiments of the invention are illustrated by way of example. It is to be expressly understood that the description and drawings are only for

purposes of illustration and as an aid to understanding, and are not intended to be a definition of the limits of the invention.

5 Detailed Description

10 The specific example of implementation described pertains to apparatuses for exchanging signals over a link between two ICs, the link being capable of propagating electrical signals.

15 Figure 1 shows an apparatus 100 suitable for transmitting signals over a link between two ICs 112. In a non-limiting example, the link between two ICs 112 includes a backplane portion. Alternatively, link 112 is a link between two ICs on a same circuit pack. As depicted, the apparatus 100 comprises an input 114, an output 116, a processing unit 102, and a transmit interface 110.

20 The input 114 is for receiving payload data from one or more functional processing units. The payload data may be in any suitable format. The functional processing units may reside on the same physical structure as apparatus 100 or on a different physical structure. In a non-limiting example, the physical structure is an electronic circuit such as an ASIC (Application Specific Integrated Circuit). The specific functional processing units from which the data originates does not form part of the invention and as
25 such will not be described.

30 The processing unit 102 processes the payload data in the input signal received at input 114 to derive associated

forward error correction data. The processing unit then generates an output signal comprising the payload data and the generated forward error correction data.

5 The interface 110 receives the output signal generated by the processing unit 102 and performs any necessary processing for transmitting the output signal over the link between two ICs 112. This may include for example multiplexing from a parallel bus to a serial bit stream.

10 The functionality of processing unit 102 will now be described in accordance with a specific example of implementation with reference to figure 2 of the drawings.

15 In accordance with a specific implementation, as depicted in figure 2, the processing unit 102 includes a set of N forward error correction (FEC) calculator units 200 202 204 206, a bit-multiplexor 208 and a framing pattern generator 210.

20 In a typical interaction, a signal including payload is received by processing unit 102 from input 114. The skilled person in the art will readily appreciate that different types of payload data may be received from port
25 114 without detracting from the spirit of the invention.

30 The payload data may be comprises of N channels or of a single channel. This specific example considers the case where the input signal is comprises of N channels. Each of the N channels is directed to a respective FEC calculator unit 200 202 204 206. At each FEC calculator unit, forward error correction data is computed on the basis of payload

data. Many different FEC schemes may be used here. In a very specific example of implementation, the FEC scheme is a 1st order Binary BCH code. Advantageously, this FEC scheme allows the FEC decoder at the receiver to correct up to 1 error per primary data structure. Each FEC calculator unit then generates a primary data structure. Each primary data structure comprises a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion. A representation of a specific implementation of the primary data structure is depicted in figure 3. In the specific implementation depicted in figure 3, each primary data structure includes 1176 bits. In the primary data structure 300, the payload data 302 occupies bits 1-1164, the forward error correction data 304 occupies 12 bits namely bits 1165-1176.

In this fashion a set of N primary data structures is generated by the set of N FEC calculator units. In a variant, the N primary data structures may be generated serially by taking N sequential portions of the payload data received at input 114 on a same channel. In this variant, a single FEC calculator unit may be used. The N primary data structures are then transmitted to the bit-multiplexor unit 208.

The bit-multiplexor unit 208 bit-multiplexes the set of N primary data structures to generate a compound data structure. A representation of a specific implementation of the primary data structure is depicted in figure 4. The compound data structure 408 shown in figure 4 is derived by

bit-multiplexing a set of $N=4$ primary data structures 400 402 404 and 406 similar in format to primary data structure 300. The skilled person in the art will readily appreciate that N can take on a plurality of non-negative integer number values greater than 0. In a non-limiting example, N is selected from the set consisting of $\{1, 2, 3, \dots, 14, 15, 16\}$. As shown, the compound data structure comprises payload data and forward error correction data. More specifically, the compound data structure comprises 582 bytes (582 8-bit words) of payload data and 6 bytes of forward error correction data 414. The manner in which the bit-multiplexor multiplexes the primary data structure may vary widely from one implementation to the other.

The table below shows a non-limiting specific implementation of the bit-multiplexing mapping.

| Compound data structure Bit numbering | Bits mapped from the 4 channels |
|--|--|
| Bit #1 | bit 1,3 ... 1175 of primary data structure #1 |
| Bit #2 | bit 1,3,... 1175 of primary data structure #2 |
| Bit #3 | bit 1,3,... 1175 of primary data structure #3 |
| Bit #4 | bit 1,3,... 1175 of primary data structure #4 |
| Bit #5 | |

| Compound data structure Bit numbering | Bits mapped from the 4 channels |
|--|--|
| | bit 2,4,... 1176 of primary data structure #1 |
| Bit #6 | bit 2,4,... 1176 of primary data structure #2 |
| Bit #7 | bit 2,4,... 1176 of primary data structure #3 |
| Bit #8 | bit 2,4,... 1176 of primary data structure #4 |

On the basis of the above table, word #1 identified as element 410 in figure 4, comprises of bits #1 and #2 of the primary data structures 400 402 404 and 406, while word #2 identified as element 412 in figure 4, comprises of bits #3 and #4 of the same primary data structures. Advantageously, bit multiplexing allows a burst of bit errors to be spread amongst the interleaved primary data structures, therefore increasing the likelihood that a given primary data structure will have no more than 1 bit error.

The compound data structure is then transmitted to the frame generation unit 210. The frame generation unit 210 generates a sequence of frames at least in part on the basis of the compound data structures received from the bit-multiplexor unit 208. Each frame includes a framing pattern and a plurality of sequential blocks, each block being characterized by a compound data structure. For each

K blocks, a framing pattern identifying frame boundaries is added. The framing pattern may be in any suitable format.

Figure 5 shows a specific example of a digital signal frame format providing forward error correction. The frame 500 and includes 66 compound data structure blocks 510 and a framing pattern 512. Each block 510 in the frame 500 is characterized by a compound data structure of the type depicted in figure 4. At the beginning of each frame, a framing pattern is appended and is designated with reference numeral 512. It will be readily apparent that the framing pattern may alternatively be appended anywhere in the frame without detracting from the spirit of the invention. The framing pattern 512 occupies 72 bytes and is a fixed pattern used to identify frame boundaries. The frames generated by the frame generation unit are then forwarded to the transmit interface 110.

The transmit interface 110 releases a signal including a sequence of frames at the output 116 for transmission over the link between two ICs 112, each frame including a plurality of sequential blocks, each block being characterized by a compound data structure suitable for carrying payload data and overhead information. The compound data structure is derived by bit-multiplexing a set of N primary data structures, each primary data structure having a first portion and a second portion. The first portion of the primary data including payload data and the second portion including forward error correction data derived from the data elements in the first portion.

In a specific example of implementation, the signal carrying the frame 500 over link between two ICs 112 has a rate of about 2.5Gb/s. The expression about 2.5Gb/s may be used to include line rates in the ranges between about 2 Gb/s and about 3 Gb/s, between about 2.4 Gb/s and about 2.8 Gb/s and between about 2.5 Gb/s and about 2.7 Gb/s. In this example, each frame in the transmitted signal has a duration of about 125 μ s.

Figure 6 shows an apparatus 600 suitable for receiving signals from the link between two ICs 112. As depicted, the apparatus 600 comprises an input 616, an output 614, a processing unit 602, and a receive interface 610.

The receive interface 610 receives the signal originating from the link between two ICs 112 and performs any necessary processing for transmitting the output signal to the processing unit 602. The signal received has a rate of about 2.5 Gb/s and comprises a sequence of frames. The receive interface 610 performs any necessary conversions between the signal on the link between two ICs 112 and the signal to be received by the processing unit 602. In a specific implementation, the receive interface 610 applies to the signal the inverse processing operation that was applied by the transmit interface 110 of figure 1. In a non-limiting example, the receive interface 110 may provide amplification, equalization, decision circuitry to translate analog voltage level to binary 1 or 0 and clock recovery circuit, amongst others.

The processing unit 602 processes the signal received from the receive interface 110 to extract payload data to

be transmitted to one or more functional processing units. The output 614 is for transmitting payload data extracted by the processing unit 602 to one or more functional processing units.

5

The functionality of processing unit 602 will now be described in accordance with a specific example of implementation with reference to figure 7 of the drawings.

10

In accordance with a specific implementation, as depicted in figure 7, the processing unit 602 includes a set of N forward error correction (FEC) processing units 700 702 704 706, a bit de-multiplexor unit 708 and a frame extraction unit 710.

15

The frame extraction unit 710 is suitable for receiving a signal including frames of the type depicted in figure 5. The frame extraction unit 710 locks in on the framing pattern in order to determine frame boundaries and block boundaries, each block being characterized by a compound data structure. The framing pattern is then removed from the frame and the blocks are forwarded to the bit de-multiplexor 708.

20

25

The bit de-multiplexor unit 708 applies to each compound data structure the inverse of the multiplexing operation applied by the bit multiplexor unit 208 shown in figure 2 in order to derive N primary data structures.

30

In the specific example depicted in the drawings, the compound data structure of the type shown in figure 4 is bit de-multiplexed into a set of N=4 primary data

structures similar in format to primary data structure 300. The skilled person in the art will readily appreciate that N can take on a plurality of non-negative integer number values greater than 0. In a non-limiting example, N is selected from the set consisting of {1, 2, 3, . . . , 14, 15, 16}. Each primary data structure comprises a first portion and a second portion, the first portion including payload data, the second portion including forward error correction data derived from the data elements in the first portion.

Each of the N primary data structures is then forwarded to a respective forward error correction (FEC) processing unit. This specific example considers the case where the payload data is associated to N channels. In a variant, where the N primary data structures include data originating from a same channel, a single FEC processing unit may be used and the N primary data structures are forwarded to the same FEC processing unit.

The FEC processing units 700 702 704 706 receive respective primary data structures. Each FEC processing unit decodes the FEC portion of the primary data structure and effects any required correction to the payload data portion. The specific FEC decoding function applied by the FEC processing units is dependent upon the FEC coding used by FEC calculator units 200 202 204 and 206. Advantageously, the use of FEC over a link between two ICs allows a reduction in the bit error rate (BER) when transmitting a signal over a backplane or between two ICs on a same circuit pack. The FEC processing units 700 702 704 706 then release a signal including payload data to output 614. The skilled person in the art will readily appreciate that different types of payload data may be

released at output 614 without detracting from the spirit of the invention.

The above-described apparatuses 100 600 for generating and receiving a signal of the type described in connection with figure 5 can be implemented on devices including a microprocessor 802 and a memory 803 as shown in figure 8. The microprocessor 802 is adapted to execute a program element 806 in order to implement the functional blocks described in the specification and depicted in the drawings. Alternatively, the above-described apparatuses 100 600 can be implemented on a dedicated hardware platform where electrical/electronic components implement the functional blocks described in the specification and depicted in the drawings.

The apparatuses 100 may form part of an integrated circuit imbedded in a dedicated chip or may form part of an IC.

It is to be appreciated that although the reception and transmission capabilities have been described with reference to figures 1 and 6 as implemented by separate apparatuses, it will be readily apparent that a same apparatus including both transmission and reception capability falls within the scope of the invention.

Although the present invention has been described in considerable detail with reference to certain preferred embodiments thereof, variations and refinements are possible without departing from the spirit of the

invention. Therefore, the scope of the invention should be limited only by the appended claims and their equivalents.

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129
130
131
132
133
134
135
136
137
138
139
140
141
142
143
144
145
146
147
148
149
150
151
152
153
154
155
156
157
158
159
160
161
162
163
164
165
166
167
168
169
170
171
172
173
174
175
176
177
178
179
180
181
182
183
184
185
186
187
188
189
190
191
192
193
194
195
196
197
198
199
200
201
202
203
204
205
206
207
208
209
210
211
212
213
214
215
216
217
218
219
220
221
222
223
224
225
226
227
228
229
230
231
232
233
234
235
236
237
238
239
240
241
242
243
244
245
246
247
248
249
250
251
252
253
254
255
256
257
258
259
260
261
262
263
264
265
266
267
268
269
270
271
272
273
274
275
276
277
278
279
280
281
282
283
284
285
286
287
288
289
290
291
292
293
294
295
296
297
298
299
300
301
302
303
304
305
306
307
308
309
310
311
312
313
314
315
316
317
318
319
320
321
322
323
324
325
326
327
328
329
330
331
332
333
334
335
336
337
338
339
340
341
342
343
344
345
346
347
348
349
350
351
352
353
354
355
356
357
358
359
360
361
362
363
364
365
366
367
368
369
370
371
372
373
374
375
376
377
378
379
380
381
382
383
384
385
386
387
388
389
390
391
392
393
394
395
396
397
398
399
400
401
402
403
404
405
406
407
408
409
410
411
412
413
414
415
416
417
418
419
420
421
422
423
424
425
426
427
428
429
430
431
432
433
434
435
436
437
438
439
440
441
442
443
444
445
446
447
448
449
450
451
452
453
454
455
456
457
458
459
460
461
462
463
464
465
466
467
468
469
470
471
472
473
474
475
476
477
478
479
480
481
482
483
484
485
486
487
488
489
490
491
492
493
494
495
496
497
498
499
500
501
502
503
504
505
506
507
508
509
510
511
512
513
514
515
516
517
518
519
520
521
522
523
524
525
526
527
528
529
530
531
532
533
534
535
536
537
538
539
540
541
542
543
544
545
546
547
548
549
550
551
552
553
554
555
556
557
558
559
560
561
562
563
564
565
566
567
568
569
570
571
572
573
574
575
576
577
578
579
580
581
582
583
584
585
586
587
588
589
590
591
592
593
594
595
596
597
598
599
600
601
602
603
604
605
606
607
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
632
633
634
635
636
637
638
639
640
641
642
643
644
645
646
647
648
649
650
651
652
653
654
655
656
657
658
659
660
661
662
663
664
665
666
667
668
669
670
671
672
673
674
675
676
677
678
679
680
681
682
683
684
685
686
687
688
689
690
691
692
693
694
695
696
697
698
699
700
701
702
703
704
705
706
707
708
709
710
711
712
713
714
715
716
717
718
719
720
721
722
723
724
725
726
727
728
729
730
731
732
733
734
735
736
737
738
739
740
741
742
743
744
745
746
747
748
749
750
751
752
753
754
755
756
757
758
759
760
761
762
763
764
765
766
767
768
769
770
771
772
773
774
775
776
777
778
779
780
781
782
783
784
785
786
787
788
789
790
791
792
793
794
795
796
797
798
799
800
801
802
803
804
805
806
807
808
809
810
811
812
813
814
815
816
817
818
819
820
821
822
823
824
825
826
827
828
829
830
831
832
833
834
835
836
837
838
839
840
841
842
843
844
845
846
847
848
849
850
851
852
853
854
855
856
857
858
859
860
861
862
863
864
865
866
867
868
869
870
871
872
873
874
875
876
877
878
879
880
881
882
883
884
885
886
887
888
889
890
891
892
893
894
895
896
897
898
899
900
901
902
903
904
905
906
907
908
909
910
911
912
913
914
915
916
917
918
919
920
921
922
923
924
925
926
927
928
929
930
931
932
933
934
935
936
937
938
939
940
941
942
943
944
945
946
947
948
949
950
951
952
953
954
955
956
957
958
959
960
961
962
963
964
965
966
967
968
969
970
971
972
973
974
975
976
977
978
979
980
981
982
983
984
985
986
987
988
989
990
991
992
993
994
995
996
997
998
999
1000
1001
1002
1003
1004
1005
1006
1007
1008
1009
1010
1011
1012
1013
1014
1015
1016
1017
1018
1019
1020
1021
1022
1023
1024
1025
1026
1027
1028
1029
1030
1031
1032
1033
1034
1035
1036
1037
1038
1039
1040
1041
1042
1043
1044
1045
1046
1047
1048
1049
1050
1051
1052
1053
1054
1055
1056
1057
1058
1059
1060
1061
1062
1063
1064
1065
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075
1076
1077
1078
1079
1080
1081
1082
1083
1084
1085
1086
1087
1088
1089
1090
1091
1092
1093
1094
1095
1096
1097
1098
1099
1100
1101
1102
1103
1104
1105
1106
1107
1108
1109
1110
1111
1112
1113
1114
1115
1116
1117
1118
1119
1120
1121
1122
1123
1124
1125
1126
1127
1128
1129
1130
1131
1132
1133
1134
1135
1136
1137
1138
1139
1140
1141
1142
1143
1144
1145
1146
1147
1148
1149
1150
1151
1152
1153
1154
1155
1156
1157
1158
1159
1160
1161
1162
1163
1164
1165
1166
1167
1168
1169
1170
1171
1172
1173
1174
1175
1176
1177
1178
1179
1180
1181
1182
1183
1184
1185
1186
1187
1188
1189
1190
1191
1192
1193
1194
1195
1196
1197
1198
1199
1200
1201
1202
1203
1204
1205
1206
1207
1208
1209
1210
1211
1212
1213
1214
1215
1216
1217
1218
1219
1220
1221
1222
1223
1224
1225
1226
1227
1228
1229
1230
1231
1232
1233
1234
1235
1236
1237
1238
1239
1240
1241
1242
1243
1244
1245
1246
1247
1248
1249
1250
1251
1252
1253
1254
1255
1256
1257
1258
1259
1260
1261
1262
1263
1264
1265
1266
1267
1268
1269
1270
1271
1272
1273
1274
1275
1276
1277
1278
1279
1280
1281
1282
1283
1284
1285
1286
1287
1288
1289
1290
1291
1292
1293
1294
1295
1296
1297
1298
1299
1300
1301
1302
1303
1304
1305
1306
1307
1308
1309
1310
1311
1312
1313
1314
1315
1316
1317
1318
1319
1320
1321
1322
1323
1324
1325
1326
1327
1328
1329
1330
1331
1332
1333
1334
1335
1336
1337
1338
1339
1340
1341
1342
1343
1344
1345
1346
1347
1348
1349
1350
1351
1352
1353
1354
1355
1356
1357
1358
1359
1360
1361
1362
1363
1364
1365
1366
1367
1368
1369
1370
1371
1372
1373
1374
1375
1376
1377
1378
1379
1380
1381
1382
1383
1384
1385
1386
1387
1388
1389
1390
1391
1392
1393
1394
1395
1396
1397
1398
1399
1400
1401
1402
1403
1404
1405
1406
1407
1408
1409
1410
1411
1412
1413
1414
1415
1416
1417
1418
1419
1420
1421
1422
1423
1424
1425
1426
1427
1428
1429
1430
1431
1432
1433
1434
1435
1436
1437
1438
1439
1440
1441
1442
1443
1444
1445
1446
1447
1448
1449
1450
1451
1452
1453
1454
1455
1456
1457
1458
1459
1460
1461
1462
1463
1464
1465
1466
1467
1468
1469
1470
1471
1472
1473
1474
1475
1476
1477
1478
1479
1480
1481
1482
1483
1484
1485
1486
1487
1488
1489
1490
1491
1492
1493
1494
1495
1496
1497
1498
1499
1500
1501
1502
1503
1504
1505
1506
1507
1508
1509
1510
1511
1512
1513
1514
1515
1516
1517
1518
1519
1520
1521
1522
1523
1524
1525
1526
1527
1528
1529
1530
1531
1532
1533
1534
1535
1536
1537
1538
1539
1540
1541
1542
1543
1544
1545
1546
1547
1548
1549
1550
1551
1552
1553
1554
1555
1556
1557
1558
1559
1560
1561
1562
1563
1564
1565
1566
1567
1568
1569
1570
1571
1572
1573
1574
1575
1576
1577
1578
1579
1580
1581
1582
1583
1584
1585
1586
1587
1588
1589
1590
1591
1592
1593
1594
1595
1596
1597
1598
1599
1600
1601
1602
1603
1604
1605
1606
1607
1608
1609
1610
1611
1612
1613
1614
1615
1616
1617
1618
1619
1620
1621
1622
1623
1624
1625
1626
1627
1628
1629
1630
1631
1632
1633
1634
1635
1636
1637
1638
1639
1640
1641
1642
1643
1644
1645
1646
1647
1648
1649
1650
1651
1652
1653
1654
1655
1656
1657
1658
1659
1660
1661
1662
1663
1664
1665
1666
1667
1668
1669
1670
1671
1672
1673
1674
1675
1676
1677
1678
1679
1680
1681
1682
1683
1684
1685
1686
1687
1688
1689
1690
1691
1692
1693
1694
1695
1696
1697
1698
1699
1700
1701
1702
1703
1704
1705
1706
1707
1708
1709
1710
1711
1712
1713
1714
1715
1716
1717
1718
1719
1720
1721
1722
1723
1724
1725
1726
1727
1728
1729
1730
1731
1732
1733
1734
1735
1736
1737
1738
1739
1740
1741
1742
1743
1744
1745
1746
1747
1748
1749
1750
1751
1752
1753
1754
1755
1756
1757
1758
1759
1760
1761
1762
1763
1764
1765
1766
1767
1768
1769
1770
1771
1772
1773
1774
1775
1776
1777
1778
1779
1780
1781
1782
1783
1784
1785
1786
1787
1788
1789
1790
1791
1792
1793
1794
1795
1796
1797
1798
1799
1800
1801
1802
1803
1804
1805
1806
1807
1808
1809
1810
1811
1812
1813
1814
1815
1816
1817
1818
1819
1820
1821
1822
1823
1824
1825
1826
1827
1828
1829
1830
1831
1832
1833
1834
1835
1836
1837
1838
1839
1840
1841
1842
1843
1844
1845
1846
1847
1848
1849
1850
1851
1852
1853
1854
1855
1856
1857
1858
1859
1860
1861
1862
1863
1864
1865
1866
1867
1868
1869
1870
1871
1872
1873
1874
1875
1876
1877
1878
1879
1880
1881
1882
1883
1884
1885
1886
1887
1888
1889
1890
1891
1892
1893
1894
1895
1896
1897
1898
1899
1900
1901
1902
1903
1904
1905
1906
1907
1908
1909
1910
1911
1912
1913
1914
1915
1916
1917
1918
1919
1920
1921
1922
1923
1924
1925
1926
1927
1928
1929
1930
1931
1932
1933
1934
1935
1936
1937
1938
1939
1940
1941
1942
1943
1944
1945
1946
1947
1948
1949
1950
1951
1952
1953
1954
1955
1956
1957
1958
1959
1960
1961
1962
1963
1964
1965
1966
1967
1968
1969
1970
1971
1972
1973
1974
1975
1976
1977
1978
1979
1980
1981
1982
1983
1984
1985
1986
1987
1988
1989
1990
1991
1992
1993
1994
1995
1996
1997
1998
1999
2000
2001
2002
2003
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2019
2020
2021
2022
2023
2024
2025
2026
2027
2028
2029
2030
2031
2032
2033
2034
2035
2036
2037
2038
2039
2040
2041
2042
2043
2044
2045
2046
2047
2048
2049
2050
2051
2052
2053
2054
2055
2056
2057
2058
2059
2060
2061
2062
2063
2064
2065
2066
2067
2068
2069
2070
2071
2072
2073
2074
2075
2076
2077
2078
2079
2080
2081
2082
2083
2084
2085
2086
2087
2088
2089
2090
2091
2092
2093
2094
2095
2096
2097
2098
2099
2100
2101
2102
2103
2104
2105
2106
2107
2108
2109
2110
2111
2112
2113
2114
2115
2116
2117
2118
2119
2120
2121
2122
2123
2124
2125
2126
2127
2128
2129
2130
2131
2132
2133
2134
2135
2136
2137
2138
2139
2140
2141
2142
2143
2144
2145
2146
2147
2148
2149
2150
2151
2152
2153
2154
2155
2156
2157
2158
2159
2160
2161
2162
2163
2164
2165
2166
2167
2168
2169
2170
2171
2172
2173
2174
2175
2176
2177
2178
2179
2180
2181
2182
2183
2184
2185
2186
2187
2188
2189
2190
2191
2192
2193
2194
2195
2196
2197
2198
2199
2200
2201
2202
2203
2204
2205
2206
2207
2208
2209
2210
2211
2212
2213
2214
2215
2216
2217
2218
2219
2220
2221
2222
2223
222